IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2841
Examiner: Yuriy Semenenko
Confirmation No.: 4886

In Re PATENT APPLICATION Of:

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|---|---|---|
| Applicant: | Seiichiro SASAKI et al. | ) |
| Serial No.: | 10/812,962 | ) |
| Filed: | March 31, 2004 | ) AMENDMENT |
| For: | Multilayered Power Supply Line for Semiconductor Integrated Circuit and Layout Method thereof | ) |
| Attny Ref.: | OKI 417 | ) |

September 20, 2006

09/21/2006 MAHMED1 00000110 10812962
01 FC:1251 120.00 OP

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This paper is in response to the Official Action mailed on May 23, 2006. Payment for one month's extension of time is attached. Please charge our Deposit Account No. 18-0002 if any additional fees are needed to enter this paper, and please advise us accordingly. It is noted that no petition is required because of the authorization to charge, but this paper is a petition for extension of time.

New claims 16 and 18 are supported at page 12, line 8, while new claims 17 and 19 are supported by the dot-dash line in instant Figs. 1 and 7. The other claims are supported in the drawing. The specification is amended to include the same language as the claims.

New claim 21 is like claim 1 but uses "consisting of" instead of "comprising" in the preamble and recites electrical connections. It is supported in the drawing.

New claim 23 is supported in the paragraph starting on page 9, as amended.

FEE ENCLOSED:$ [illegible]
Please charge any further fee to our Deposit Account No. 18-0002